WEST

Generate Collection | Print

Search Results - Record(s) 1 through 8 of 8 returned.

☐ 1. Document ID: US 4860191 A

L2: Entry 1 of 8 File: USPT Aug 22, 1989

US-PAT-NO: 4860191
DOCUMENT-IDENTIFIER: US 4860191 A

TITLE: Coprocessor with dataflow circuitry controlling sequencing to execution unit of data received in tokens from master processor

L2: Entry 1 of 8 File: USPT Aug 22, 1989

US-PAT-NO: 4860191
DOCUMENT-IDENTIFIER: US 4860191 A

TITLE: Coprocessor with dataflow circuitry controlling sequencing to execution unit of data received in tokens from master processor

DATE-ISSUED: August 22, 1989

INT-CL: [4] G06F 15/16, G06F 15/20, G06F 13/38

US-CL-ISSUED: 364/200
US-CL-CURRENT: 710/110; 712/201

FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 4811345 A

L2: Entry 2 of 8 File: USPT Mar 7, 1989

US-PAT-NO: 4811345
DOCUMENT-IDENTIFIER: US 4811345 A

TITLE: Methods and apparatus for providing a user oriented microprocessor test interface for a complex, single chip, general purpose central processing unit

L2: Entry 2 of 8 File: USPT Mar 7, 1989

US-PAT-NO: 4811345
DOCUMENT-IDENTIFIER: US 4811345 A

TITLE: Methods and apparatus for providing a user oriented microprocessor test interface for a complex, single chip, general purpose central processing unit

DATE-ISSUED: March 7, 1989

INT-CL: [4] G06F 11/00

US-CL-ISSUED: 371/16; 364/200
US-CL-CURRENT: 714/27

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3631405	December 1971	Hoff et al.	395/650
☐	4276594	June 1981	Morley	395/800
☐	4541048	September 1985	Propster et al.	395/375
☐	4594651	June 1986	Jaswa et al.	364/131
☐	4641238	February 1987	Kneib	395/290
☐	4799144	January 1989	Parruck et al.	364/200
☐	4811345	March 1989	Johnson	395/183.03
☐	4860191	August 1989	Nomura et al.	395/290
☐	4862407	August 1989	Fette et al.	395/800
☐	4876660	October 1989	Owen et al.	364/754
☐	4908825	March 1990	Vea	370/110.3
☐	4975947	December 1990	Chauvel	379/334
☐	4991169	February 1991	Davis et al.	370/77
☐	5005168	April 1991	Cummiskey et al.	370/24
☐	5029204	July 1991	Shenoi et al.	379/407
☐	5036539	July 1991	Wrench, Jr. et al.	395/2.55
☐	5045993	September 1991	Murakami et al.	395/375
☐	5111530	May 1992	Kutaragi et al.	395/2.79
☐	5155852	October 1992	Murakami et al.	395/725
☐	5185599	February 1993	Doornink et al.	395/143
☐	5208832	May 1993	Greiss	364/715.11
☐	5293586	March 1994	Yamazaki et al.	395/164

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
299537	January 1989	EPX	

OTHER PUBLICATIONS

MCS 8080/8085 Family User's Manual, Intel 1986, 5-1-19.
MCS 80/85 Family User's Manual, Intel Corporation, 1986, Chapter 5, The Instruction Set.
Electronic Design, Aug. 22, 1991, Microcontroller Eases Closed-Loop Servo Control, Dave Bursky, pp. 119-121.
National Semiconductor, Jan. 1990, NS32FX16-15/NS32FX-16-20/NS32FX16-25, High Performance FAX Processor.
Electronic Engineering Times, Aug. 26, 1991.; Ron Wilson: "Zilog Uses DSP for Disk Drive IC".
National Semiconductor, Jan. 11, 1989, KV96-X6D modem chip set.
"A Next-Generation 32 bit VLSI Signal Processor"; Shinjo Tsujimichi et al.; ICASSP 86, Tokio; 1986 IEEE; pp. 415-416.
Wescon Technical Papers, 30th Oct. 1984, pp. 4/3/1-7; Perlman: Bipolar and CMOS Technologies Become Partners in Dig. Sig. Processing.
IEEE Micro, vol. 6, No. 6, Dec. 1986, pp. 60-69; Eichen: "NEC'S mu PD77230 Digital Signal Processor".
Electronics, vol. 52, No. 26, Dec. 1979, pp. 109-115; Schirm: "Packing a signal

processor onto a single digital board".
Texas Instruments, "TMS320C25 User's Guide Preliminary"; pp. 1/1-1/5, 2/1-2/21.
Doi et al., "A digital signal processor for modem applications", Electronic Engineer, Oct. 1989, pp. 198-204, 206.
Rockwell Preliminary Data Sheet, "R96DFX 9600bps Monofax Modem with Error Detection and DTMF Reception", Document #29200N60; Jul. 1989.
Yamaha Preliminary Data Sheet, "YM7109 MD96FX (9600bps Fax Modem LSI)", Catalog No.:LSI.
Reiner, et al.; "VLSI Development of a Global Memory Interface Controller"; pp. 0254-0257 (7.8.1.-7.8.4.); IEEE 1990.
Ruby B. Lee; "HP Precision: A Spectrum Architecture"; pp. 242-251; IEEE 1989.
Sorin Iacobovici; "A Pipelined Interface for High Floating-Point Performance with Precise Exceptions"; pp. 77-87; IEEE 1988.
Fotland et al.; "Hardware Design of the First HP Precision Architecture Computers"; pp. 4-17; Hewlett Packard Journal Mar., 1987.
R. Haines: "Two muCs on one chip split the silicon and the work": Electronic Design, vol. 29, No. 10, May 1981, pp. 197-202, Waseca, US.
L. Vieira et al.: "A multiprocessing system for the TMS32020": Microprocessing and Microprogramming: vol. 23, nos. 1-5, Mar. 1988, pp. 221-225 Amsterdam, NL.
M.C. Ertem: "A reconfigurable co-processor for microprocessor systems": Conference Proceedings of the IEEE Sourtheastcon '87:Tampa, Florida, 5th-8th, Apr. 1987, fol. 1, pp. 225-228, IEEE.
M. Homewood et al.: "The IMS T800 transputer": IEEE Micro, vol. 7, No. 5, Oct. 1987, pp. 10-26.
J.R. Schweitzer: "Design implementation and analysis of a modular digital signal processing system": 5th International Conference on Systems Engineering: Fairborn, Ohio, 9th-11th; Sep. 1987, pp. 447-450, IEEE, New York, US.
M.L. Fuccio et al: "The DSP32C: AT&T's second-generation floating-point digital signal processor": IEEE Micro, vol. 8, No. 6, Dec. 1988, pp. 30-47, IEEE, New York, US.

ART-UNIT: 232
PRIMARY-EXAMINER: Pan; Daniel H.
ATTY-AGENT-FIRM: Limbach & Limbach L.L.P.

ABSTRACT:

An integrated data processing platform for processing a digital signal that includes a general purpose processor and a digital signal processor (DSP) module. The DSP module recovers digital data from a digital signal utilizing a sequence of DSP operations selected by the general purpose processor. The general purpose processor processes the digital data recovered by the DSP module, but is also available to perform general purpose tasks. A shared internal memory array selectively provides information to the DSP module and to the general purpose processor. The information stored in the internal memory array includes operands utilized in the execution of the DSP algorithm and selected instructions and data utilized by the general purpose CPU either for controlling the execution of the DSP algorithm or for executing its own general purpose tasks. While in many applications the data processing system will include an analog front end that converts a modulated input signal received on an analog transmission channel to a corresponding digital signal for processing by the data processing system, the data processing system may also receive the digital signal directly from a digital source.

10 Claims, 11 Drawing figures

FIELD-OF-SEARCH: 371/15, 371/16, 371/17, 371/18, 371/20, 324/73R, 324/73AT, 364/2MSFile

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC
Draw. Desc | Image

☐ 3. Document ID: US 4799144 A

L2: Entry 3 of 8 File: USPT Jan 17, 1989

US-PAT-NO: 4799144
DOCUMENT-IDENTIFIER: US 4799144 A

TITLE: Multi-function communication board for expanding the versatility of a computer

L2: Entry 3 of 8 File: USPT Jan 17, 1989

US-PAT-NO: 4799144
DOCUMENT-IDENTIFIER: US 4799144 A

TITLE: Multi-function communication board for expanding the versatility of a computer

DATE-ISSUED: January 17, 1989

INT-CL: [4] G06F 3/16

US-CL-ISSUED: 364/200; 379/284
US-CL-CURRENT: 710/2; 379/284, 379/387.01, 379/88.01, 379/88.07, 379/908, 704/275, 712/33, 712/38, 712/43

FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile, 381/36-40, 340/825.19, 179/6.08, 179/6.06, 179/18BC, 179/18G, 379/88, 379/89, 379/96, 379/284, 379/97

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC
Draw. Desc | Image

☐ 4. Document ID: US 4641238 A

L2: Entry 4 of 8 File: USPT Feb 3, 1987

US-PAT-NO: 4641238
DOCUMENT-IDENTIFIER: US 4641238 A

TITLE: Multiprocessor system employing dynamically programmable processing elements controlled by a master processor

L2: Entry 4 of 8 File: USPT Feb 3, 1987

US-PAT-NO: 4641238
DOCUMENT-IDENTIFIER: US 4641238 A

TITLE: Multiprocessor system employing dynamically programmable processing elements controlled by a master processor

DATE-ISSUED: February 3, 1987

INT-CL: [4] G06F 15/16

US-CL-ISSUED: 364/200
US-CL-CURRENT: 710/110; 902/2, 902/39

FIELD-OF-SEARCH: 364/200, 364/900

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 5. Document ID: US 4594651 A

L2: Entry 5 of 8 File: USPT Jun 10, 1986

US-PAT-NO: 4594651
DOCUMENT-IDENTIFIER: US 4594651 A

TITLE: Concurrent processor for control

L2: Entry 5 of 8 File: USPT Jun 10, 1986

US-PAT-NO: 4594651
DOCUMENT-IDENTIFIER: US 4594651 A

TITLE: Concurrent processor for control

DATE-ISSUED: June 10, 1986

INT-CL: [4] G06F 9/00

US-CL-ISSUED: 364/131; 364/180
US-CL-CURRENT: 700/2

FIELD-OF-SEARCH: 364/131, 364/135, 364/2MSFile, 364/180, 364/160, 364/704, 318/590, 318/596

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 6. Document ID: US 4541048 A

L2: Entry 6 of 8 File: USPT Sep 10, 1985

US-PAT-NO: 4541048
DOCUMENT-IDENTIFIER: US 4541048 A

TITLE: Modular programmable signal processor

L2: Entry 6 of 8 File: USPT Sep 10, 1985

US-PAT-NO: 4541048
DOCUMENT-IDENTIFIER: US 4541048 A

TITLE: Modular programmable signal processor

DATE-ISSUED: September 10, 1985

INT-CL: [3] G06F 7/38, G06F 15/00

US-CL-ISSUED: 364/200; 364/736
US-CL-CURRENT: 712/32; 708/524

FIELD-OF-SEARCH: 364/200, 364/736

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 7. Document ID: US 4276594 A

L2: Entry 7 of 8 File: USPT Jun 30, 1981

US-PAT-NO: 4276594
DOCUMENT-IDENTIFIER: US 4276594 A

TITLE: Digital computer with multi-processor capability utilizing intelligent composite memory and input/output modules and method for performing the same

L2: Entry 7 of 8 File: USPT Jun 30, 1981

US-PAT-NO: 4276594
DOCUMENT-IDENTIFIER: US 4276594 A

TITLE: Digital computer with multi-processor capability utilizing intelligent composite memory and input/output modules and method for performing the same

DATE-ISSUED: June 30, 1981

INT-CL: [3] G06F 15/16, G06F 13/00

US-CL-ISSUED: 364/200
US-CL-CURRENT: 713/600

FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 8. Document ID: US 3631405 A

L2: Entry 8 of 8 File: USPT Dec 28, 1971

US-PAT-NO: 3631405
DOCUMENT-IDENTIFIER: US 3631405 A

TITLE: SHARING OF MICROPROGRAMS BETWEEN PROCESSORS

L2: Entry 8 of 8 File: USPT Dec 28, 1971

US-PAT-NO: 3631405
DOCUMENT-IDENTIFIER: US 3631405 A

TITLE: SHARING OF MICROPROGRAMS BETWEEN PROCESSORS

DATE-ISSUED: December 28, 1971

INT-CL: [] G06f 9/12, G06f 15/16

US-CL-ISSUED: 340/172.5
US-CL-CURRENT: 712/209; 709/310, 709/312, 712/226, 712/229, 712/246, 712/247

FIELD-OF-SEARCH: 340/172.5

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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Term	Documents
"3631405".USPT.	1
3631405S	0
"4276594".USPT.	1
4276594S	0
"4541048".USPT.	1
4541048S	0
"4594651".USPT.	1
4594651S	0
"4641238".USPT.	1
4641238S	0
"4799144".USPT.	1
(3631405.PN. OR 4276594.PN. OR 4541048.PN. OR 4594651.PN. OR 4641238.PN. OR 4799144.PN. OR 4811345.PN. OR 4860191.PN.).USPT.	8

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Search Results - Record(s) 1 through 10 of 10 returned.

☐ 1. Document ID: US 6175912 B1

L5: Entry 1 of 10 File: USPT Jan 16, 2001

US-PAT-NO: 6175912
DOCUMENT-IDENTIFIER: US 6175912 B1

TITLE: Accumulator read port arbitration logic

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

☐ 2. Document ID: US 5911082 A

L5: Entry 2 of 10 File: USPT Jun 8, 1999

US-PAT-NO: 5911082
DOCUMENT-IDENTIFIER: US 5911082 A

TITLE: Parallel processing building block chip

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

☐ 3. Document ID: US 5812562 A

L5: Entry 3 of 10 File: USPT Sep 22, 1998

US-PAT-NO: 5812562
DOCUMENT-IDENTIFIER: US 5812562 A

TITLE: Low cost emulation scheme implemented via clock control using JTAG controller in a scan environment

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

☐ 4. Document ID: US 5727194 A

L5: Entry 4 of 10 File: USPT Mar 10, 1998

US-PAT-NO: 5727194
DOCUMENT-IDENTIFIER: US 5727194 A

TITLE: Repeat-bit based, compact system and method for implementing zero-overhead loops

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 5. Document ID: US 5619514 A

L5: Entry 5 of 10 File: USPT Apr 8, 1997

US-PAT-NO: 5619514
DOCUMENT-IDENTIFIER: US 5619514 A

TITLE: In-place present state/next state registers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 6. Document ID: US 5559837 A

L5: Entry 6 of 10 File: USPT Sep 24, 1996

US-PAT-NO: 5559837
DOCUMENT-IDENTIFIER: US 5559837 A

TITLE: Efficient utilization of present state/next state registers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 7. Document ID: US 5465275 A

L5: Entry 7 of 10 File: USPT Nov 7, 1995

US-PAT-NO: 5465275
DOCUMENT-IDENTIFIER: US 5465275 A

TITLE: Efficient utilization of present state/next state registers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 8. Document ID: JP 62097062 A

L5: Entry 8 of 10 File: JPAB May 6, 1987

PUB-NO: JP362097062A
DOCUMENT-IDENTIFIER: JP 62097062 A
TITLE: DIGITAL SIGNAL PROCESSOR

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 9. Document ID: JP 10143364 A

L5: Entry 9 of 10 File: DWPI May 29, 1998

DERWENT-ACC-NO: 1998-367366
DERWENT-WEEK: 199832

TITLE: Digital signal processor - has processor core and user circuit on single chip by which un-registered user instruction and registered user instruction are decoded and executed

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Clip Img | Image

☐ 10. Document ID: CN 1174353 A, DE 19735348 A1, FR 2752965 A1, JP 10116268 A, US 5838984 A, TW 345650 A, KR 98018072 A, KR 236527 B1

L5: Entry 10 of 10 File: DWPI Feb 25, 1998

DERWENT-ACC-NO: 1998-170237
DERWENT-WEEK: 200171

TITLE: Digital signal parallel vector processor for multimedia applications - has single instruction multiple data processor using several banks of vector registers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Clip Img | Image

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Term	Documents
SINGLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1985971
SINGLES.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1792
INSTRUCTION$	0
INSTRUCTION.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	208503
INSTRUCTIONA.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	26
INSTRUCTIONABLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
INSTRUCTIONADDRESS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2
INSTRUCTIONADDRESSER.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
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INSTRUCTIONAL.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	6780
(SINGLE NEAR4 INSTRUCTION$ NEAR9 (DSP OR DIGITAL NEAR1 SIGNAL) NEAR10 REGISTER$).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	10

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Term	Documents
SINGLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1985971
SINGLES.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1792
INSTRUCTION$	0
INSTRUCTION.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	208503
INSTRUCTIONA.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	26
INSTRUCTIONABLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
INSTRUCTIONADDRESS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2
INSTRUCTIONADDRESSER.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
INSTRUCTIONAI.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
INSTRUCTIONAL.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	6780
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Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

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DATE: Monday, February 25, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L5	single near4 instruction$ near9 (dsp or digital near1 signal) near10 register$	10	L5
L4	L3 and general near1 purpose	77	L4
L3	single near4 instruction$ near9 (dsp or digital near1 signal)	160	L3
DB=USPT; PLUR=YES; OP=OR			
L2	3631405.pn. or 4276594.pn. or 4541048.pn. or 4594651.pn. or 4641238.pn. or 4799144.pn. or 4811345.pn. or 4860191.pn.	8	L2
DB=EPAB; PLUR=YES; OP=OR			
L1	299537	1	L1

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Search Results -

Term	Documents
SINGLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1985971
SINGLES.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1792
INSTRUCTION$	0
INSTRUCTION.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	208503
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INSTRUCTIONABLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
INSTRUCTIONADDRESS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2
INSTRUCTIONADDRESSER.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
INSTRUCTIONAI.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
INSTRUCTIONAL.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	6780
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(SINGLE NEAR4 INSTRUCTION$ NEAR9 (DSP OR DIGITAL NEAR1 SIGNAL) NEAR10 REGISTER$).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	10

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Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L5

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Search History

DATE: Monday, February 25, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L5	single near4 instruction$ near9 (dsp or digital near1 signal) near10 register$	10	L5
L4	L3 and general near1 purpose	77	L4
L3	single near4 instruction$ near9 (dsp or digital near1 signal)	160	L3
DB=USPT; PLUR=YES; OP=OR			
L2	3631405.pn. or 4276594.pn. or 4541048.pn. or 4594651.pn. or 4641238.pn. or 4799144.pn. or 4811345.pn. or 4860191.pn.	8	L2
DB=EPAB; PLUR=YES; OP=OR			
L1	299537	1	L1

END OF SEARCH HISTORY

WEST

End of Result Set

Generate Collection | Print

L1: Entry 1 of 1 File: USPT May 13, 1997

US-PAT-NO: 5630153
DOCUMENT-IDENTIFIER: US 5630153 A

TITLE: Integrated digital signal processor/general purpose CPU with shared internal memory

DATE-ISSUED: May 13, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Intrater; Amos	Lantau			HKX
Doron; Moshe	Sunnyvale	CA		
Intrater; Gideon	Ramat-Gan			ILX
Epstein; Lev	Holon			ILX
Valentaten; Maurice	Geldtendorf			DEX
Greiss; Israel	Raanana			ILX

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
National Semiconductor Corporation	Santa Clara	CA			02

APPL-NO: 8/ 317783 [PALM]
DATE FILED: October 4, 1994

PARENT-CASE:
This is a continuation of application Ser. No. 08/011,102 filed on Jan. 29, 1993, now abandoned, which is a continuation of application Ser. No. 07/467,148 filed on Jan. 18, 1990 now abandoned.

INT-CL: [6] G06 F 9/26, G06 F 9/40, G06 F 9/44, G06 F 13/36

US-CL-ISSUED: 395/800; 395/290, 395/306, 364/DIG.1, 364/DIG.2
US-CL-CURRENT: 712/35; 710/110, 712/36

FIELD-OF-SEARCH: 395/800, 395/290, 395/200.01, 395/375, 395/200.03, 395/700, 395/289, 395/287, 395/297, 395/2.79, 395/183.19, 395/2.55, 395/775, 395/306, 364/DIG.1, 364/DIG.2, 364/706, 364/736, 364/726

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

WEST

End of Result Set

Generate Collection Print

L1: Entry 1 of 1 File: EPAB Jan 18, 1989

PUB-NO: EP000299537A2
DOCUMENT-IDENTIFIER: EP 299537 A2
TITLE: Apparatus and Method for processing digital signal.

PUBN-DATE: January 18, 1989

INVENTOR-INFORMATION:

NAME	COUNTRY
FUKUDA, MITUYOSHI	
SHIMIZU, MASAHISA	
OHASHI, HIDEKI	
KAWAGUCHI, MASAKI	

ASSIGNEE-INFORMATION:

NAME	COUNTRY
SANYO ELECTRIC CO	JP

APPL-NO: EP88111551
APPL-DATE: July 18, 1988

PRIORITY-DATA: JP00334688A (January 11, 1988), JP17930187A (July 17, 1987), JP19489487A (August 4, 1987)

INT-CL (IPC): G06F 15/00
EUR-CL (EPC): G06F015/78; G06F017/10

ABSTRACT:

CHG DATE=19990617 STATUS=O> An apparatus for processing a digital signal includes a pair of data buses (11), a pair of digital processing circuits (12, 13) respectively connected to corresponding one of the data buses, and a control circuit (20) which simultaneously controls the digital processing circuits. To the digital processing circuits, an external storage including cyclic storage areas is connected. The digital processing circuits evaluate an actual address data for the cyclic storage areas of the external storage by means of predetermined arithmetic operation. The actual address data is outputted through the data buses and an external storage interface circuit (16) to the external storage. An address data being stored in a storage of the digital processing circuit is read. During one instruction cycle, the read address data is incremented or decremented, and when the result thereof is a boundary of the cyclic storage areas, a predetermined value is outputted from an ALU (28). A starting address is added to the predetermined value and a result thereof is outputted as the actual address data.